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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Shih

Group Art Unit: 3743
Examiner: L. Ciric

Serial No.: 09/410,896

Filed: Oct 2, 1999

For: Apparatus and Method For Cooling A Semiconductor Substrate

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Attorney Docket No.: 67,200-207

EXPRESS MAIL CERTIFICATE

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I hereby certify that this paper in triplicate and a credit card payment form in the amount of $320.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Box Appeal, Assistant Commissioner for Patents, Washington, D.C. 20231

Kathy Dixon

***REVISED* APPEAL BRIEF**

Box Appeal
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Appellants appeal in the captioned application from the Examiner's final rejection, dated November 6, 2001, of claims 16, 18 and 20 under 35 USC §102(e) as being anticipated by Flanigan et al and of claims 1-3, 5, 8-10, 12-16 and 18-20, under 35 USC §103(a) as being unpatentable over Moslehi.

It is urged that the rejections be reversed and that all the claims be allowed.

The separate rejection of claim 12 under 35 USC §112 is not contested.

(1) REAL PARTY IN INTEREST

The real party in interest in the present appeal is the recorded Assignee of Taiwan Semiconductor Manufacturing Company, Ltd.

(2) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that are known to the Appellant, the Appellant's legal representative, or the assignee.

(3) STATUS OF CLAIMS

Claims 1-3, 5, 8-10, 12-16 and 18-20 are pending in the application.

Claims 1-3, 5, 8-10, 12-16 and 18-20 stand rejected.

(4) STATUS OF AMENDMENTS

A Request For Reconsideration was filed on or about January 3, 2002 which contained claim amendments.

An Advisory Action mailed February 26, 2002 by the Examiner which denied entering of the amendments.

(5) SUMMARY OF THE INVENTION

The invention is directed to a cooling stage 70 for holding a semiconductor substrate that is provided with a plurality of circular grooves 74 concentrically formed in a top surface of the stage 70 and a plurality of linear grooves 36 formed in radial directions emanating from a center 80 of the top surface 72 in fluid communication with the plurality of circular grooves 74 such that a cooling fluid flows through the grooves 36,74 to improve cooling of the underside of a substrate placed on the stage 70 and a method for cooling a semiconductor substrate.

(Specification, page 7, lines 5-10)

The first plurality may be at least three and the second plurality may be at least two, or the first plurality may be preferably five and the second plurality may be preferably three. The first plurality of circular grooves 74 and the second plurality of linear grooves 36 each may have a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm, or each may have a width preferably between about 3 mm and about 5 mm, and a depth preferably between about 1 mm and about 3 mm.

(6) ISSUES

Issue I

Is the rejection of claims 16, 18 and 20 under 35 USC §102(e) as being anticipated by Flanigan et al proper when such reference does not teach the specifically claimed limitation in the present application?

Issue II

Is the rejection of claims 1-3, 5, 8-10, 12-15 and 19 under 35 USC §103(a) as being unpatentable over Moslehi '745 proper when such reference does not teach or suggest the specifically claimed limitations in the present application?

(7) GROUPING OF CLAIMS

The rejection of claims 1-3, 5, 8-10, 12-16 and 18-20 are contested as a group.

(8) ARGUMENTS

Issue I

Claims 16, 18 and 20 are rejected under 35 USC §102(e) as being anticipated by Flanigan et al. It is contended that Flanigan et al discloses the invention essentially as claimed, including a wafer pedestal 104 characterized by five circular concentric

grooves and a plurality of linear radial grooves in fluid communication with each and every one of the circular concentric grooves **to enable cooling using a coolant** which may be argon.

The Appellants respectfully submit that the rejection of claims 16, 18 and 20 under 35 USC §102(e) based on Flanigan et al is improper and must be reversed.

Flanigan et al discloses an apparatus for improved biasing and retaining of a workpiece in a workpiece processing system. At col. 4, line 66+:

> "The gas conduit 142 extends vertically from the bottom of the shaft 126 to the bottom surface 202 of the electrostatic chuck 105 to **allow a heat transfer gas to be pumped under the wafer during processing**. A detailed depiction of the gas conduit 142 interfacing with the bottom surface 202 of the electrostatic chuck 105 is seen in Fig. 5 ..."

Furthermore, at col. 5, lines 22-23:

> "The heat transfer gas is pumped from one or more remote sources 130 and 134 of Fig. 1 which is connected to a second end of the gas conduit 142 via ..."

The Appellants respectfully submit that the surface grooves shown by Flanigan et al in Fig. 2 in the top surface 103 of the electrostatic chuck 105 is not used for cooling at all, instead, the grooves are used for achieving heat transfer on the wafer backside, thus achieving a more uniform wafer temperature. This is a well-known, standard process step for a semiconductor plasma processor that is equipped with an electrostatic chuck. The surface grooves provided by Flanigan et al are therefore not used to "enable cooling using a coolant" as suggested by the Examiner. As a matter of fact, the cooling of the electrostatic chuck 105 is achieved instead by a plurality of grooves 236 in the cooling plate 234 shown in Fig. 2. As stated at col. 6, lines 15+:

> "In a preferred embodiment of the invention, the electrode has the form of a cooling plate 234 fabricated of a block of copper or stainless steel ... The cooling plate 234 has a top surface 235.

> The top surface may have a plurality of grooves 236. **The grooves 236 reduce the surface area of the top surface 235 of the cooling plate 234 that is in contact with the electrostatic chuck 105** such that the amount of heat extracted from the chuck (and wafer) is moderated. The size and number of the grooves 236 may be of any dimension, amount or configuration so as to achieve the desired cooling effect of the plate 234."

The Appellants therefore respectfully submit that the rejection of claims 16, 18 and 20 under 35 USC §102(e) based on Flanigan et al is improper and must be reversed.

Issue II

Claims 1-3, 5, 8-10, 12-16 and 18-20 are rejected under 35 USC §103(a) as being unpatentable over Moslehi.

Claims 1-3, 5, 8-10, 12-15 and 19 are rejected under 35 USC §103(a) as being unpatentable over Moslehi.

In the Response To Arguments section of the 11/06/01 Office Action, the Examiner notes that the Appellants' argument that the Moslehi reference does not clearly teach, disclose or

suggest a second plurality of linear grooves that are in fluid communication with each and every one of a first plurality of circular grooves, is not valid. The Examiner cited Figure 3 of Moslehi and col. 7, lines 3-15 of the same reference. The Examiner further argued that the term "a first plurality of circular grooves" is subjected to broad interpretation and therefore, may mean only the innermost two concentric circular grooves, as shown in Figure 3 of Moslehi.

The rejection of claims 1-3, 5, 8-10, 12-16 and 18-20 under 35 USC §103(a) based on Moslehi is improper and must be reversed.

The Appellants respectfully submit that the interpretation of the claim language is guided by the specification, including the drawings. Furthermore, dependent claims 2 and 3 define the term "first plurality" to be at least 3 (claim 2) or at least 5 (claim 3). Therefore, by interpreting the dependent claims, the specification and the drawings, the term "first plurality" necessarily indicates all the circular grooves provided on the surface of the pedestal which would include all three circular grooves shown by Moslehi in Figure 3. The Appellants therefore respectfully submit that Moslehi does not teach fluid communication between a second plurality of linear

grooves with "each and everyone of said first plurality of circular grooves" to allow a cooling fluid to flow therethrough.

Claim 1 further recites:

> "said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm."

The Appellants respectfully submit that such is not taught or disclosed by Moslehi. Similar limitations are contained in independent method claim 8.

As the Court stated in W.L. Gore and Associates, Inc., v. Garlock, Inc.,721 F2d 1540, 220 USPQ 303 (Fed.Cir. 1983):

> "To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher."

The rejection of claims 1-3, 5, 8-10, 12-16 and 18-20 under 35 USC §103(a) based on Moslehi is improper and must be reversed.

CLOSING

In summary, the Appellants have shown that their claimed invention is fully supported by a body of evidence of non-anticipation and non-obviousness. It is therefore respectfully submitted that such evidence of non-anticipation and non-obviousness overcomes any showing of anticipation and obviousness presented by the Examiner. The Appellants therefore submit that the final rejection of their claims 1-3, 5, 8-10, 12-16 and 18-20 is improper under 35 USC §102(e) and §103(a).

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Tung & Associates

By: _____

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Telephone: (248) 540-4040

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CLAIM APPENDIX

1. A cooling stage for a semiconductor substrate comprising:

a pedestal having a substantially planar top surface,

a first plurality of circular grooves concentrically formed in said top surface, and

a second plurality of linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with each and everyone of said first plurality of circular grooves allowing a cooling fluid to flow therethrough when said semiconductor substrate is positioned on said top surface of the pedestal, said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm.

2. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality is at least three and said second plurality is at least two.

3. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality is at least five and said second plurality is at least three.

5. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 3 mm and about 5 mm, and a depth between about 1 mm and about 3 mm.

8. A method for cooling a semiconductor substrate comprising the steps of:

providing a cooling stage comprising a wafer pedestal equipped with a grooved top surface thereon, said grooved top surface comprises a first plurality of circular grooves concentrically formed in said top surface and a second plurality of linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with each and everyone of said first plurality of circular grooves, said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm,

positioning a heated semiconductor substrate on said grooved top surface,

flowing a cooling liquid through a cooling channel in said wafer pedestal to carry away heat transferred to said grooved top surface, and

flowing a cooling gas through said first and second plurality of circular and linear grooves to carry away heat from a backside of said heated semiconductor substrate.

9. A method for cooling a semiconductor substrate according to claim 8, wherein said first plurality of circular grooves comprises at least three circular grooves and said second plurality of linear grooves comprises at least two linear grooves.

10. A method for cooling a semiconductor substrate according to claim 8, wherein said first plurality of circular grooves comprises at least five circular grooves and said second plurality of linear grooves comprises at least three linear grooves.

12. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of providing said grooved top surface with a plurality of circular and linear grooves, each having a width between about 3 mm and about 5 mm, and a depth of between about 1 mm and about 3 mm.

13. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of positioning a semiconductor substrate exiting a high temperature sputtering chamber on said grooved top surface of said cooling stage.

14. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of removing a cooled-down semiconductor substrate from said cooling stage and positioning the substrate in a low temperature sputter chamber.

15. A method for cooling a semiconductor substrate according to claim 8 further comprising the steps of flowing a cooling liquid through said cooling channel in said wafer pedestal, and flowing a cooling gas of an inert gas through said first and second plurality of circular and linear grooves.

16. A wafer pedestal effective for cooling a high temperature processed wafer comprising:

a wafer pedestal having a substantially planar top surface,

at least three circular grooves concentrically formed in said top surface, and

at least two linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with each and everyone of said at least three circular grooves for flowing a cooling fluid therethrough cooling said high temperature processed wafer positioned thereon.

18. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said at least three circular grooves comprises at least five circular grooves and wherein said at least two linear grooves comprises at least three linear grooves.

19. A wafer pedestal effective for cooling a high temperature processed wafer according to claim 16 wherein said at least three circular grooves comprises nine circular grooves and said at least two linear grooves comprises three linear grooves each having a width of about 2 mm and a depth of about 1 mm.

20. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said cooling fluid flowing through said circular and said linear grooves is an inert gas selected from the group consisting of argon, nitrogen and helium.

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Serial No.: 09/ 410,896
Filed: Oct. 2, 1999
For: Apparatus and Method For Cooling a Semiconductor Substrate

Group Art Unit: 3743
Examiner: L. Ciric

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF *REVISED* APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on Feb. 6, 2002.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

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3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
___ small entity $160.00
___ other than a small entity $320.00
X was already paid

Appeal Brief fee due: $ 0

Certificate of Mailing/Transmission (37 CFR 1.8(a))
I hereby certify that this correspondence is, on the date shown below, being:

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X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 056 175 158 US in an envelope addressed to Box Appeal, Assistant Commissioner for Patents, Washington, D.C. 20231

Kathy Dixon

Dated: May 20, 2002

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 390.00	$195.00
☐	three months	$ 930.00	$465.00
☐	four months	$1,470.00	$735.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

__X__ was already paid

Appeal Brief Fee: $ 0
Extension fee (if any) $_____

TOTAL FEE DUE: $ 0

6. FEE PAYMENT

____ Attached is a Credit Card Payment Form for the sum of $_____
____ Charge Visa Credit Card No. 4756 8461 9568 0263 .
A duplicate copy of this transmittal is attached.

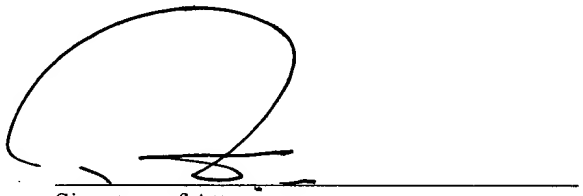
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

__X__ If any additional extension and/or fee is required, this is a request therefor to charge Visa Credit Card No. 4756 8461 9568 0263 .

And/Or

__X__ If any additional fee for claims is required, please charge Visa Credit Card No. 4756 8461 9568 0263 .



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